**PROGRAM BCA**

**SEMESTER III**

**COURSE CODE & NAME DCA2103, Computer Organization**

**SET-I**

**1. Explain von Neumann Architecture in detail.**

**Ans:**

**Structure of the IAS Computer**

IAS is the first digital computer in which the von Neumann Architecture was employed. The general structure of the IAS computer is as shown in figure

 A main memory, which stores both instructions and data

 An arithmetic and logic unit (ALU) capable of operating on binary data

 A control unit,

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**2. Explain in detail the different instruction formats with examples.**

**Ans: Instruction Formats**

Instruction Format is defined as the layout of bits in an instruction in terms of its constituent parts. An Instruction Format must include opcode implicitly or explicitly and one or more operand(s). For, most instruction sets have usually mor

**3. Discuss the organization of main memory.**

**Ans:** A memory unit is the collection of storage units or devices together. The memory unit stores the binary information in the form of bits. Generally, memory/storage is classified into 2 categories:

* **Volatile Memory**: This loses its data, when power is switched off.
* **Non-Volatile Memory**:

**SET-II**

**4. List and explain the mapping functions.**

**Ans: Mapping functions**

The correspondence between the main memory and CPU are specified by a mapping function. There are three standard mapping functions namely

**1. Direct mapping**

**2. Associative**

**5. What is an interrupt? Discuss the hardware actions in interrupt handling.**

**Ans:** An interrupt is a signal emitted by a device attached to a computer or from a program within the computer. It requires the operating system (OS) to stop and figure out what to do next. An interrupt temporarily stops or terminates a service or a current process.

With Interrupt driven I/O,

**6. Explain the characteristics of RISC and CISC architectures.**

## Ans: RISC Characteristics

Let's take a closer look at some of the characteristics of RISC one at a time.

**1. Small and Limited Numbers of Instructions**

As explained earlier, to increase the speed and performance of RISC, a limited number of frequently used instructions are executed. This reduces the number of cycles per instruction but at a cost of total number of instructions executed in the same time frame.

**2. Hardwired**