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| **SESSION** | **SEPTEMBER 2022** |
| **PROGRAM** | **MASTER of COMPUTER APPLICATIONS (MCA)** |
| **SEMESTER** | **I** |
| **course CODE & NAME** | **DCA6105 – COMPUTER ARCHITECTURE** |

**SET-I**

**1. (a) Explain the evolution of computer architecture with the help of different generations.**

**Ans: Zeroth Generation Computers:** The zeroth generation of computers (1642-1946) was distinctly made available by the invention of largely mechanical computers. In 1642, a French mathematician named Blaise Pascal invented the first mechanical device which was called Pascaline. In 1822, Charles Babbage, an English mathematician, invented a machine

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**(b) How is parallelism different from concurrent execution? Explain Flynn’s classification in detail.**

**Ans: Concurrent execution** is the temporal behaviour of the N-client 1-server model where one client is served at any given moment. This model has a dual nature; it is sequential in a small time scale, but simultaneous in a rather large time scale. In this situation, the key problem is how the competing clients, let us say processes or threads, should be scheduled for

**2. (a) Explain zero, one, two and three address instruction with the help of given instruction X=(A\*B)/C+(D+E)\*F**

**(b) What are the different types of addressing modes? Explain all.**

**Ans: The following are the different types of address modes:**

**Implied Mode:** The operands in this mode are specified implicitly in the explanation of the instruction.

**For example,** the instruction ‘‘complement accumulator’’ is considered as an implied mode instruction as the description of the instruction implies the operand in the accumulator

**3. (a) What are the different types of pipeline hazards? Explain techniques to handle hazards.**

**Ans:** Hazards are the situations that stop the next instruction in the instruction stream from being executed during its designated clock cycle. Hazards reduce the performance from the ideal speedup gained by pipelining. In general, there are three major categories of hazards

**SET-II**

**4. (a) What is mapping? Explain direct and associative mapping in detail.**

**Ans:** Mapping refers to the translation of main memory address to the cache memory address. The transfer of information from main memory to cache memory is conducted in units of cache blocks on cache lines. Blocks in caches are called block frames which are

**(b) What are vector processors? Explain types of vector processing.**

**Ans:** Vector processing is a central processing unit that can perform the complete vector input in individual instruction. It is a complete unit of hardware resources that implements a sequential set of similar data elements in the memory using individual instruction.

**5. (a) Explain fine-grained and coarse-grained SIMD architectures.**

**Ans: Fine-Grained SIMD Architecture** The Steven Unger design scheme is the initial base for the Fine-grained SIMD architectures. These are generally designed for low-level image processing applications.

 **(b) Explain UMA, NUMA, and COMA in detail.**

**Ans:** Basically the memory is divided into several modules that is why large multiprocessors into different categories. Let’s discuss them in detail. UMA (Uniform Memory Access): In this category every processor and memory module has similar access time. Hence each memory word can be read as quickly as other memory word. If not then quick references are

**6. (a) What is RAID? Explain different levels of RAID.**

**Ans: RAID** RAID is the acronym for ‘redundant array of inexpensive disks’. There are several approaches to redundancy that have different overhead and performance. The Patterson, Gibson, and Katz 1987 paper introduced the term RAID. It used a numerical

**(b) What is Multithreading? Explain the difference between process and thread.**

**Ans: Multithreading** Multithreading is the capability of a processor to do multiple things at one time. The Windows operating system uses the API (Application Programming Interface)